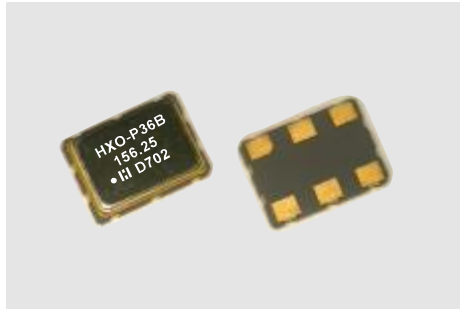


## • D7SP Series 7.0\*5.0 LV\_PECL OSC



### FEATURES

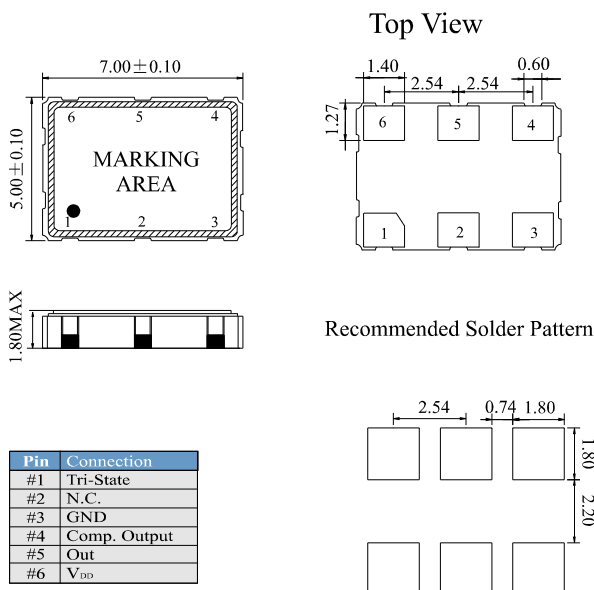
- 7.0\*5.0\*1.8mm package
- Tri-State function available
- Low Jitter and Noise
- PECL output
- Ideal for Fiber-optic communication applications, FTTH and SONET/SDH applications, Sever, FCHBA, Fibre Channel, Gigabit Ethernet, and Serial ATA

### Electrical Specifications

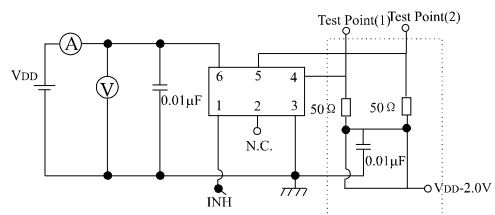
Parameter	Condition	D7SP
Frequency Range	F <sub>0</sub>	25~156.25MHz
Output Specification		LV-PECL
Frequency Stability*	All Condition	±25ppm, ±50ppm, ±100ppm
Operating Temperature Range	T <sub>OPR</sub>	-20°C~+70°C (-40°C~+85°C option)
Storage Temperature Range	T <sub>STG</sub>	-55°C~+125°C
Power supply Voltage	V <sub>DD</sub>	3.3V+/-5%      2.5V+/-5%
Supply Current	I <sub>DD</sub>	90mA Max
Output Symmetry	Sym	At ½V <sub>pp</sub> 40/60%(45/55% Option)
Rise time	T <sub>r</sub>	20%V <sub>pp</sub> ~80%V <sub>pp</sub> 1nS Max
Fall Time	T <sub>f</sub>	80%V <sub>pp</sub> ~20%V <sub>pp</sub> 1nS Max
Output Voltage	V <sub>OH</sub> V <sub>OL</sub>	V <sub>DD</sub> -1.025V Min. V <sub>DD</sub> -1.62V Max.
Output Load		50 Ω to V <sub>DD</sub> -2.0V
Integrated phase jitter (RMS)	Integrated 12KHz to 20MHz	1pS Max
Start Time	T <sub>s</sub>	10mS Max
Aging(First Year)	25°C ±3°C	±2ppm Max
Pin 1,tri-state function		Pin 1=H or open....Output active at pin 4,5 Pin 1=L.....high impedance at pin 4,5
Packing Unit		1000pcs/reel

\*Include: 25°C tolerance, operating temperature range, input voltage change, aging, load change, shock and vibration

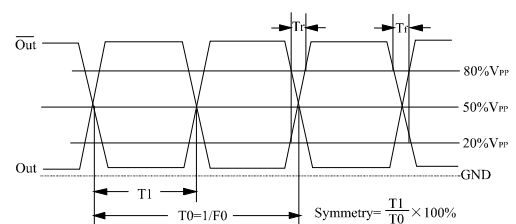
### Mechanical Dimensions(mm)



### Test Circuit



### Output Waveform



\*\*Note: 0.01 μF bypass capacitor should be placed between V<sub>DD</sub>(Pin6) and GND(Pin3) to Minimize power supply line noise